REMARKS

Applicants have canceled claims 15-31, without prejudice or disclaimer since these claims are directed to a non-elected invention. Accordingly, claims 1-14 are pending.

Applicants have provided a new title of the invention, as required. The new title should comply with the Examiner's requirement for a descriptive title of the invention.

Claims 5 and 8 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Moriyama, U.S. Patent No. 6,195,260. Further, Moriyama has been used in a rejection under 35 U.S.C. § 103(e) to reject claims 1-4, 6, 7, 9 and 10. Still further, the Examiner relies upon Moriyama as a primary reference in rejecting the claims under 35 U.S.C. § 103(e) in combination with Ishida, U.S. Patent No. 6,329,065 (claim 11), and further in view of Wolf et al (claims 12 and 14) or Zakel et al (claim 13). Reconsideration of the rejections is requested for the following reasons.

According to the present invention, Applicants have determined there are problems associated with secondary mounting reflow of surface mounted parts that are soldered to a wiring board, such as the chip part 18, shown in comparative Figs. 16 and 17. As shown in the figures, a connection

terminal 18a (Fig. 17) is plated with a solder for internal soldering that has improved solder wetability. Then, a Pb series high temperature solder having a melting point of 256°C is used for the secondary mounting reflow. In the reflow, plating Sn for the connection terminal is fused into the solder connection portion 18b to form a Pb-Sn eutectic phase, which lowers the melting point of the Pb series high temperature solder. As a result, the solder connection portion 18b is put into a re-molten state during the secondary mounting reflow. Further, since the sealing resin 20 that is used is of high hardness, the solder re-melting expansion pressure 9 in the solder connection portion 18b (Fig. 16) is increased to become higher than the resin pressure 19 to cause defoliation at the boundary between the resin 20 and the chip 18 so a solder flow out 10 is formed in the gap as shown in Figs. 16 and 17, resulting in a short-circuit failure.

According to the present invention, the outflow of solder 10, as shown in Fig. 16 and 17, is prevented by using a particular resin, specifically a low elasticity resin 6 having a modulus of elasticity of 1 MPa or more at a temperature of 25°C. The elastic insulative resin covers the surface mounted parts that are mounted by the internal soldering on the wiring

substrate and the solder connection portions that connect the surface mounted parts to the wiring substrate. Preferably, the elastic resin is a resin having a modulus of elasticity of 200 MPa or less at a temperature of 150°C or higher as set forth on page 6, lines 1-10 of the specification, for example.

In accordance with the present invention, even when the internal solder connection parts are melted again upon mounting the second semiconductor device in a secondary mounting reflow procedure, the pressure caused by the melting expansion can be moderated with the elastic resin and as a result the peeling at the boundary between the surface mounted parts and the resin can be prevented as well as at the boundary between the resin and the module substrate, as set forth on page 19, lines 11-18 of the specification, for example.

The Examiner recognizes that the modulus of elasticity of an elastic resin is an inherent property of the resin. However, the reference to Moriyama does not disclose the problem of a short circuit being caused by the flow out of solder during a remelting or secondary reflow mounting procedure, as recognized by the inventors. Accordingly, Moriyama does not teach the effectiveness of controlling the

modulus of elasticity of a resin that is employed for sealing in the manner of the present invention. Accordingly, the reference does not disclose or suggest to one having ordinary skill in the art that the modulus of elasticity of the resin affects the state of the interior parts when subjected to secondary reflow soldering, as described in the present invention.

Specifically, Applicants disclose that the low elasticity resin 6 is a resin having both a protective function capable of protecting the interior parts through its mechanical strength and a flexibility capable of moderating the solder re-melting expansion pressure 9 that is discussed with reference to Fig. 16. A silicone resin (silicon rubber) A or a low elastic epoxy resin B, C or D having the modulus of elasticity shown in Fig. 5 are preferred examples of the elastic resin of the present invention. Accordingly, Moriyama does not disclose the invention as claimed by Applicants.

The Examiner relies upon Ishida et al as a secondary reference for disclosing a wire board in which the terminals are plated with gold, tin or a lead-tin alloy. However, Ishida et al do not disclose or suggest the claimed sealing portion of the semiconductor device that is formed with an

insulative resin having a modulus elasticity of 1 MPa or more and 200 MPa or less at a temperature of 150°C or more and a modulus of elasticity of 200 MPa or more at a temperature of 25°C, as set forth in base claim 9, from which claims 11-14 depend. Further, neither Zakel et al nor Wolf et al disclose or suggest the obviousness of the invention as set forth in these claims. Accordingly, claims 11-14 are patentable over each of these references whether considered individually or in combination, as proposed in the Office Action.

In view of the foregoing amendments and remarks, reconsideration and reexamination are respectfully requested.

Respectfully submitted,

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